(12) UK Patent Application (19) GB (11) 2 346 480 (13) A

(43) Date of A Publication 09.08.2000

(21) Application No 0002759.9

(22) Date of Filing 07.02.2000

(30) Priority Data
(31) 09245435 (32) 05.02.1999 (33) US

(51) INT CL[7]
H01L 33/00 // H01L 21/18 , H01S 5/10

(52) UK CL (Edition R)
H1K K1EA K1EA1 K2R3A K2S1C K2S1D K2S1E K2S16

(56) Documents Cited
GB 2333895 A GB 2307791 A EP 0896405 A
EP 0860913 A US 5804834 A

(58) Field of Search
UK CL (Edition R) H1K KEAX KELF KELQ KELX KPXDB
INT CL[7] H01L 21/18 21/20 33/00 , H01S 5/10 5/183 5/187
ONLINE:WPI, EPODOC, JAPIO

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(54) Abstract Title
A wafer bonded AlGaInN structure

(57) A device, for example a VCSEL, has an $Al_xGa_yIn_zN$ structure 18 comprising an n- type type layer and a p-type layer constituting an active layer, positioned proximate to a substrate. A first mirror stack 14, interposes the substrate 12 and a bottom side of the $Al_xGa_yIn_zN$ layer. A wafer bond interface 16, interposes the first mirror stack and a selected one of the substrate and $Al_xGa_yIn_zN$ structure. There are p and an n contacts 22a, 22b. The p contact is electrically connected to the p-type layer and the n contact is electrically connected to the n-type layer. The substrate may be made from GaP, GaAs, InP or Si. There may be an intermediate bonding layer selected from a group that includes dielectrics and alloys containing halides, ZnO, indium, tin, chrome, gold, nickel, copper, and II-VI materials. One method for fabricating the $Al_xGa_yIn_zN$ structure comprises; attaching a host substrate to a first mirror stack, fabricating an $Al_xGa_yIn_zN$ structure on a sacrificial growth substrate and creating a wafer bond interface. The sacrificial growth substrate is then removed and electrical contacts are deposited on to the $Al_xGa_yIn_zN$ structure. A second method for fabricating an $Al_xGa_yIn_zN$ structure comprises; fabricating an $Al_xGa_yIn_zN$ structure to a sacrificial growth substrate and attaching a first mirror stack on top of an $Al_xGa_yIn_zN$ structure. The host substrate is wafer bonded to the first mirror stack to create a wafer bond interface. The sacrificial growth substrate is then removed and electrical contacts are deposited on the $Al_xGa_yIn_zN$ structure. Laser melting may be used to remove the substrate.

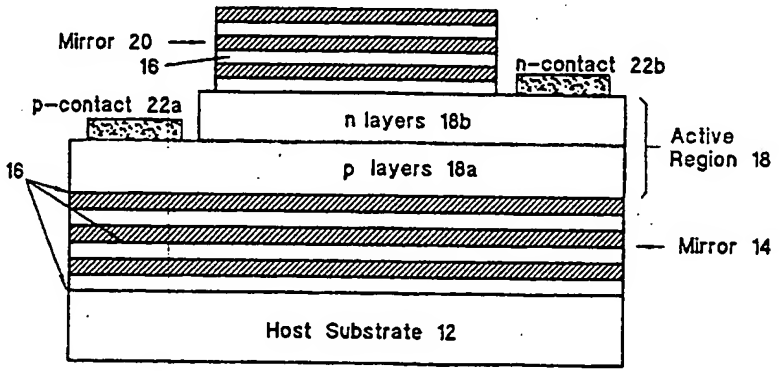

Figure 2

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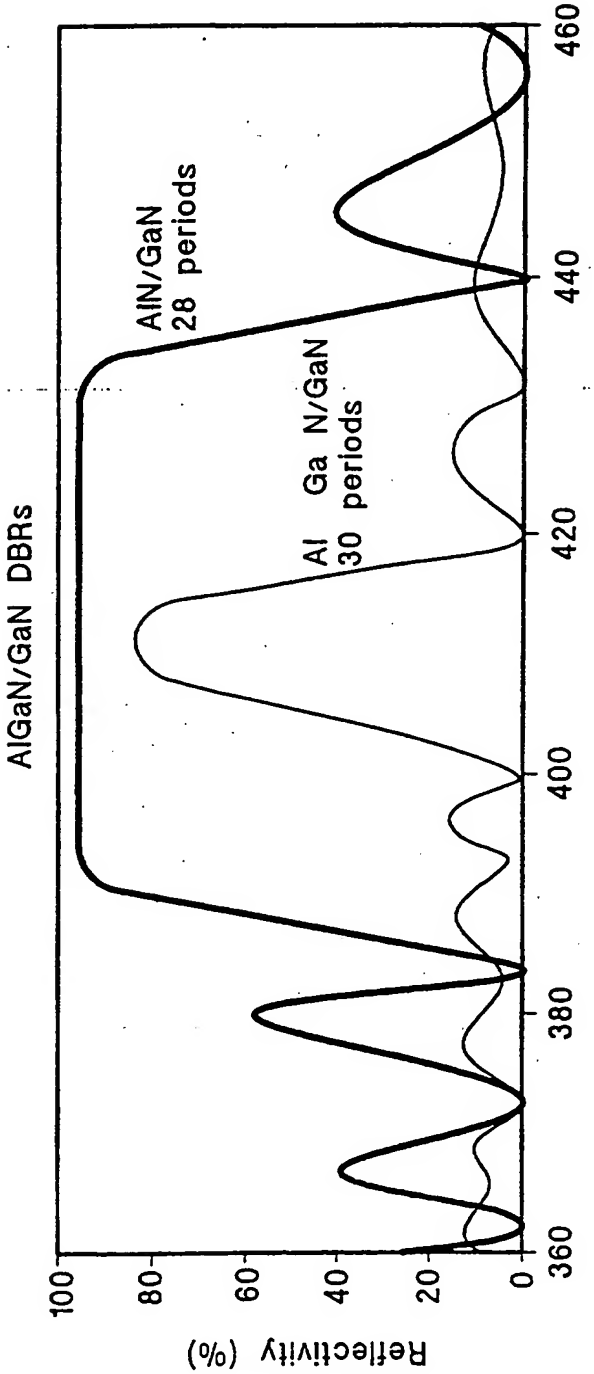

Theoretical reflectivity vs. wavelength for AlN/GaN and $Al_{.30}Ga_{.70}N$/GaN DBRs

Figure 1

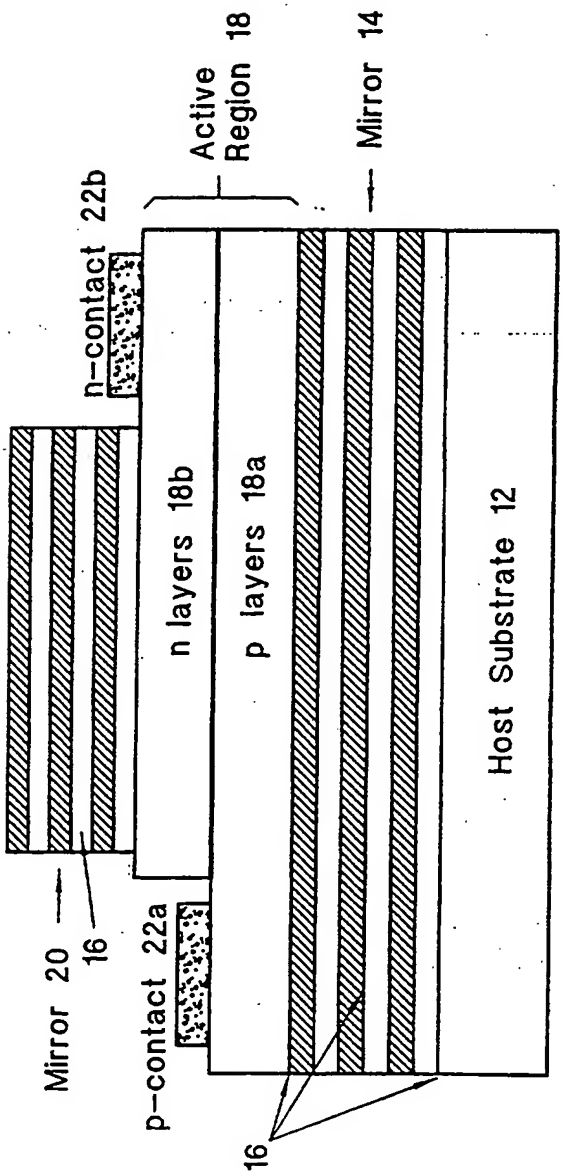
Mirror 20
16
p-contact 22a
n-contact 22b
n layers 18b
Active Region 18
p layers 18a
Mirror 14
Host Substrate 12
16

Figure 2

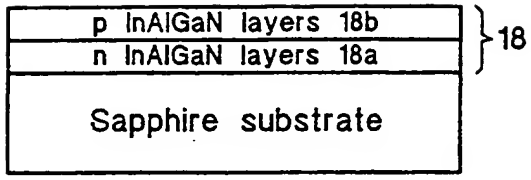

Figure 3a

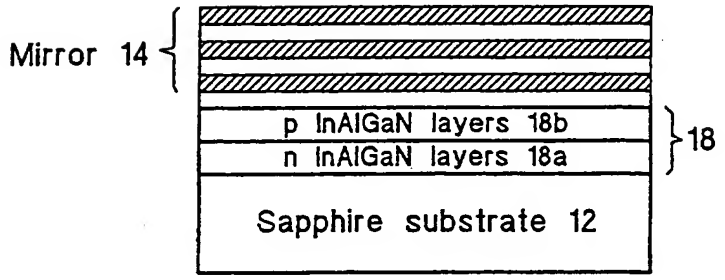

Figure 3b

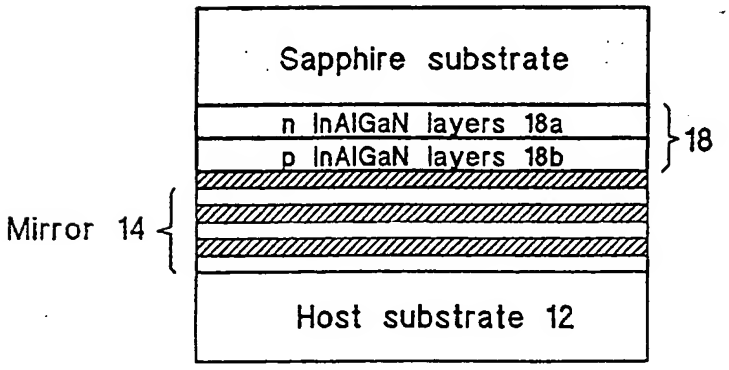

Figure 3c

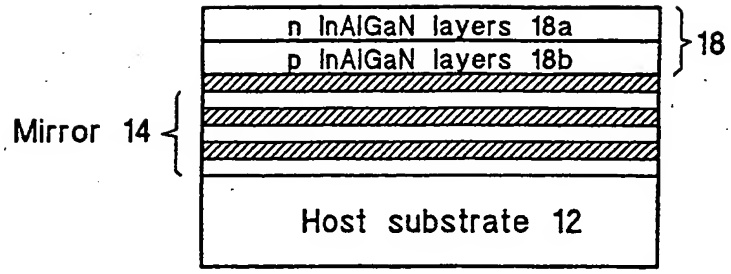

Figure 3d

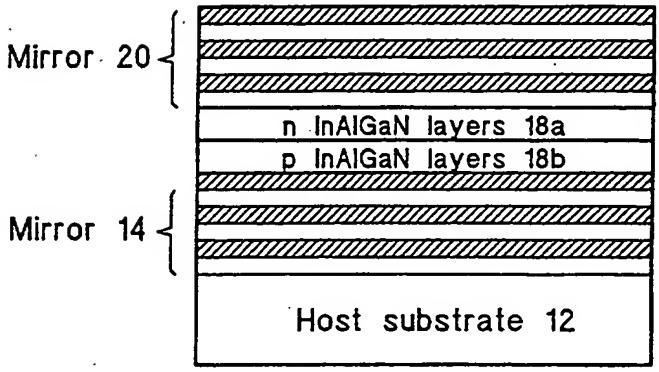

Figure 3e

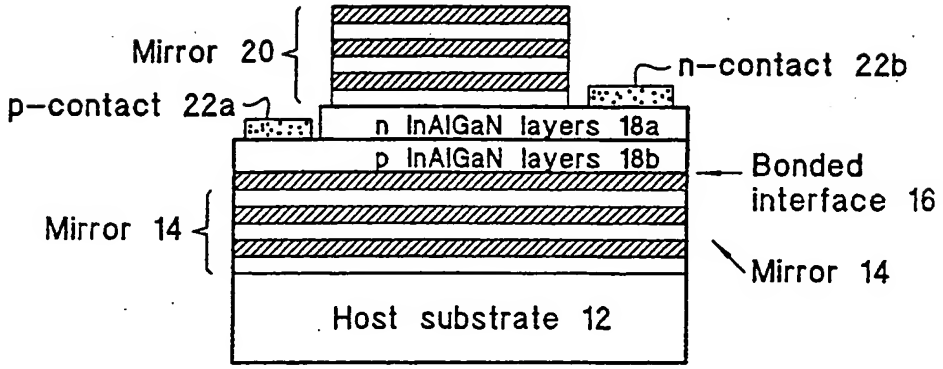

Figure 3f

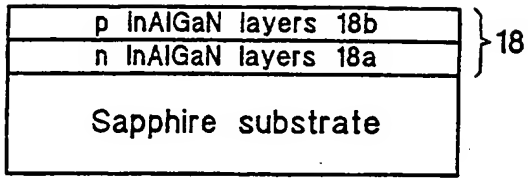

Figure 4a

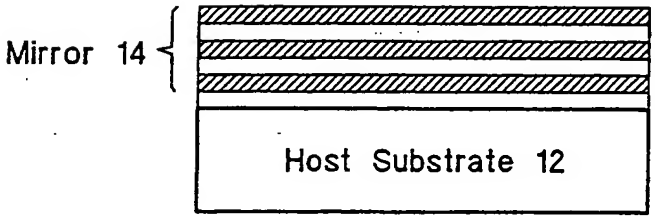

Figure 4b

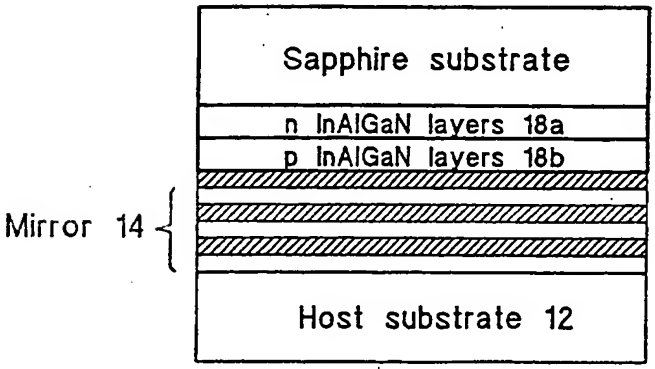

Figure 4c

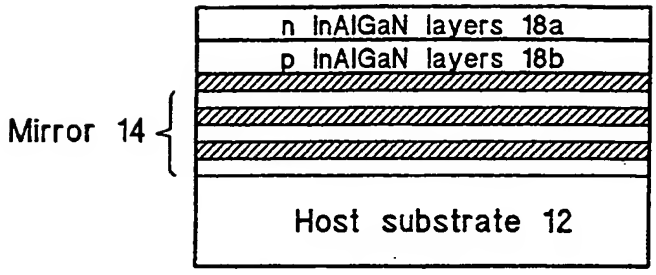

Figure 4d

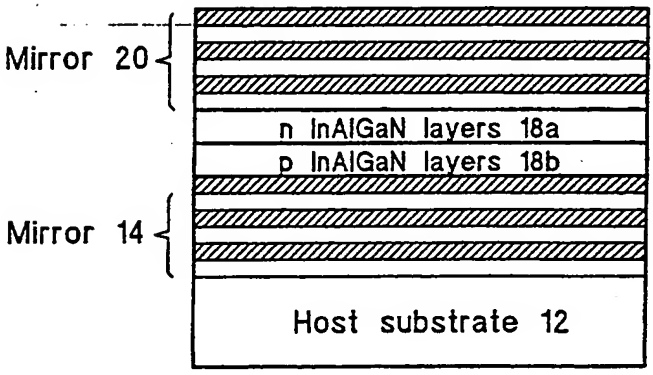

Figure 4e

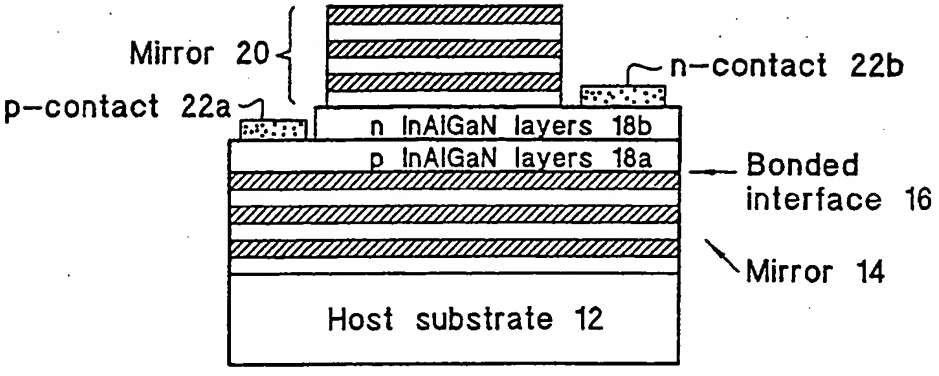

Figure 4f

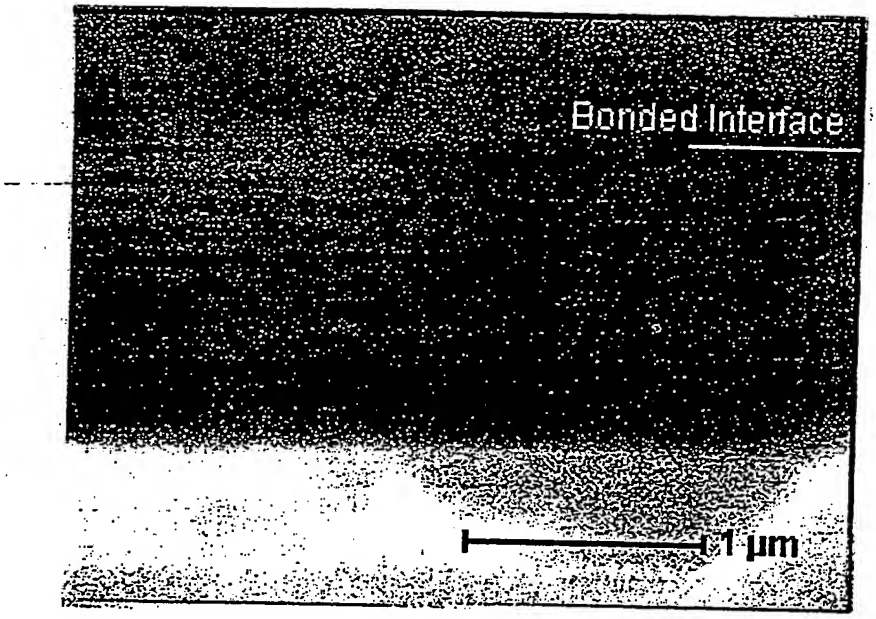

Figure 5

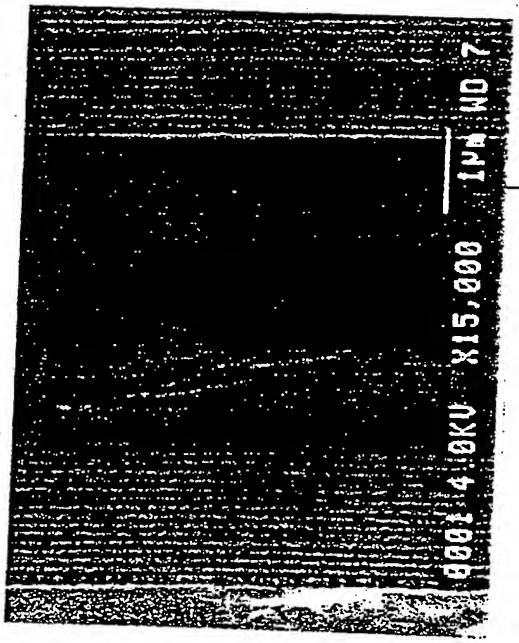

Figure 6

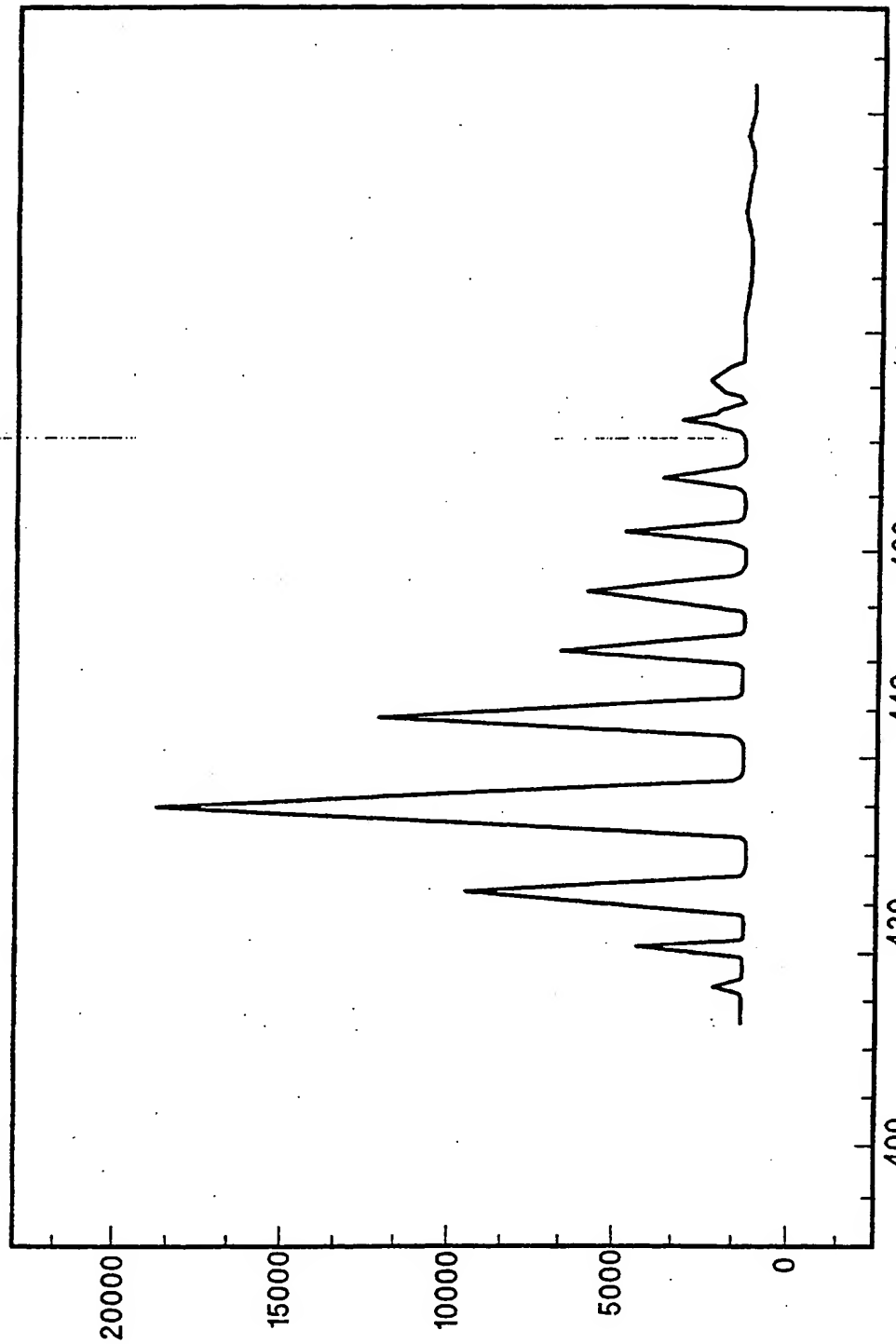
20000
15000
10000
5000
0
400
420
440
460
480
500
wavelength (nm)

Figure 7

WAFER BONDED $AL_XGA_YIN_ZN$ STRUCTURES

The invention is directed towards the field of light emission particularly towards providing high quality reflective surfaces to both sides of an $Al_xGa_yIn_zN$ device,

A vertical cavity optoelectronic structure consists of an active region that is formed by light emitting layer interposing confining layers that may be doped, un-doped, or contain a p-n junction. The structure also contains at least one reflective mirror that forms a Fabry-Perot cavity in the direction normal to the light emitting layers. Fabricating a vertical cavity optoelectronic structure in the $GaN/Al_xGa_yIn_zN/Al_xGa_{1-x}N$ (where $x+y+z=1$ in $Al_xGa_yIn_zN$ and where $x \leq 1$ in $Al_xGa_{1-x}N$) material systems poses challenges that set it apart from other III-V material systems. It is difficult to grow $Al_xGa_yIn_zN$ structures with high optical quality. Current spreading is a major concern for $Al_xGa_yIn_zN$ devices. Lateral current spreading in the p-type material is ~30 times less than that in the n-type material. Furthermore, the low thermal conductivity of many of the substrates adds complexity to the device design, since the devices should be mounted junction down for optimal heat sinking.

One vertical cavity optoelectronic structure, e.g. a vertical cavity surface emitting laser (VCSEL), requires high quality mirrors, e.g. 99.5% reflectivity. One method to achieve high quality mirrors is through semiconductor growth techniques. To reach the high reflectivity required of distributed Bragg reflectors (DBRs) suitable for VCSELs (>99%), there are serious material issues for the growth of semiconductor $Al_xGa_yIn_zN$

DBRs, including cracking and electrical conductivity. These mirrors require many periods/layers of alternating indium aluminum gallium nitride compositions ($Al_xGa_yIn_zN$ / $Al_{x'}Ga_{y'}In_{z'}N$). Dielectric DBRs (D-DBR), in contrast to semiconductor DBRs, are relatively straightforward to make with reflectivities in excess of 99% in the spectral range spanned by the $Al_xGa_yIn_zN$ system. These mirrors are typically deposited by evaporation or sputter techniques, but MBE (molecular beam epitaxial) and MOCVD (metal-organic chemical vapor deposition) can also be employed. However, only one side of the active region can be accessed for D-DBR deposition unless the growth substrate is removed. Producing an $Al_xGa_yIn_zN$ vertical cavity optoelectronic structure would be significantly easier if it was possible to bond and/or deposit D-DBRs on both sides of a $Al_xGa_yIn_zN$ active region.

Wafer bonding can be divided into two basic categories: direct wafer bonding, and metallic wafer bonding. In direct wafer bonding, the two wafers are fused together via mass transport at the bonding interface. Direct wafer bonding can be performed between any combination of semiconductor, oxide, and dielectric materials. It is usually done at high temperature (>400°C) and under uniaxial pressure. One suitable direct wafer bonding technique is described by Kish, et al., in U.S.P.N. 5,502,316. In metallic wafer bonding, a metallic layer is deposited between the two bonding substrates to cause them to adhere. One example of metallic bonding, disclosed by Yablonovitch, et al. in Applied Physics Letters, vol. 56, pp. 2419-2421, 1990, is flip-chip bonding, a technique used in the micro- and optoelectronics industry to attach a device upside down onto a substrate. Since flip-chip bonding is used to improve the heat sinking of a device, removal of the substrate depends upon the device structure and conventionally the only requirements of the metallic bonding layer are that it be electrically conductive and mechanically robust.

In "Low threshold, wafer fused long wavelength vertical cavity lasers", Applied Physics Letters, Vol. 64, No. 12, 1994, pp1463-1465, Dudley, et al. taught direct wafer bonding of AlAs/GaAs semiconductor DBRs to one side of a vertical cavity structure while in "Room-Temperature Continuous-Wave Operation of 1.54-μm Vertical-Cavity Lasers," IEEE Photonics Technology Letters, Vol. 7, No. 11, November 1995, Babic, et al. taught direct wafer bonded semiconductor DBRs to both sides of an InGaAsP VCSEL

to use the large refractive index variations between AlAs/GaAs. As will be described, wafer bonding D-DBRs to $Al_xGa_yIn_zN$ is significantly more complicated than semiconductor to semiconductor wafer bonding, and was not known previously in the art.

In "Dielectrically-Bonded Long Wavelength Vertical Cavity Laser on GaAs Substrates Using Strain-Compensated Multiple Quantum Wells," IEEE Photonics Technology Letters, Vol. 5, No. 12, December 1994, Chua et al. disclosed AlAs/GaAs semiconductor DBRs attached to an InGaAsP laser by means of a spin-on glass layer. Spin-on glass is not a suitable material for bonding in a VCSEL between the active layers and the DBR because it is difficult to control the precise thickness of spin on glass, and hence the critical layer control needed for a VCSEL cavity is lost. Furthermore, the properties of the glass may be inhomogeneous, causing scattering and other losses in the cavity.

Optical mirror growth of $Al_xGa_{1-x}N$/GaN pairs of semiconductor DBR mirrors with reflectivities adequate for VCSELs, e.g. > 99%, is difficult. Referring to Figure 1, theoretical calculations of reflectivity suggest that to achieve the required high reflectivity, a high index contrast is required that can only be provided by increasing the Al composition of the low-index $Al_xGa_{1-x}N$ layer and/or by including more layer periods (material properties taken from Ambacher et al., MRS Internet Journal of Nitride Semiconductor Research, 2(22) 1997). Either of these approaches introduces serious challenges. If current will be conducted through the DBR layers, it is important that the DBRs be conductive. To be sufficiently conductive, the $Al_xGa_{1-x}N$ layer must be adequately doped. Electrical conductivity is insufficient unless the Al composition is reduced to below approximately 50% for Si (n-type) doping and to below approximately 20% for Mg (p-type) doping. However, as shown in Figure 1, the number of layer periods needed to achieve sufficient reflectivity using lower Al composition layers requires a large total thickness of $Al_xGa_{1-x}N$ material, increasing the risk of epitaxial layer cracking (due to the relatively large lattice mismatch between AlN and GaN) and reducing compositional control. Indeed, the $Al_{.30}Ga_{.70}N$/GaN stack of Figure 1 is already ~ 2.5 μm thick and is far from sufficiently reflective for a VCSEL. Thus, a high reflectivity DBR based on this layer pair requires a total thickness significantly greater than 2.5 μm and would be difficult to grow reliably given the mismatch between AlN and

GaN growth conditions and material properties. Even though the cracking is not as great of an issue if the layers are un-doped, compositional control and the AlN/GaN growth temperatures still pose great challenges to growing high reflectivity DBRs. Hence, even in applications where the DBRs do not have to conduct current, semiconductor mirror stacks with reflectivities >99% in the $Al_xGa_yIn_zN$ material system have not been demonstrated. For this reason, dielectric-based DBR mirrors are preferred.

At least one mirror stack, e.g. a dielectric distributed Bragg reflector (D-DBR) or composite D-DBR/semiconductor DBR interposes a $Al_xGa_yIn_zN$ active region and a host substrate. A wafer bond interface is positioned somewhere between the host substrate and the active region. An optional intermediate bonding layer is adjacent the wafer bond interface to accommodate strain and thermal coefficient mismatch at the wafer bond interface. An optional mirror stack is positioned adjacent the $Al_xGa_yIn_zN$ active region. Either the host substrate or intermediate bonding layer is selected for compliancy.

One embodiment of the aforementioned invention consists of a device having the wafer bond interface positioned adjacent the $Al_xGa_yIn_zN$ active region, the $Al_xGa_yIn_zN$ active region is fabricated on a sacrificial substrate, e.g. Al_2O_3. The mirror stack attached to a host substrate is direct wafer bonded to the $Al_xGa_yIn_zN$ active region. Next, the sacrificial substrate is removed. The optional mirror stack is attached to the top of the $Al_xGa_yIn_zN$ active region. Techniques for attaching include bonding, depositing, and growing. Electrical contacts are added to the n-type and p-type layers.

For an alternate embodiment having the wafer bond interface positioned adjacent the host substrate, the mirror stack is attached on top of the $Al_xGa_yIn_zN$ active region. If direct wafer bonding is employed, a host substrate, selected to have the proper mechanical properties, is wafer bonded to the mirror stack. Alternatively, metallic bonding may be used to bond the host substrate to the mirror stack. The sacrificial substrate is removed. An optional mirror stack is attached on top of the $Al_xGa_yIn_zN$ active region. Electrical contacts are added to the n-type and p-type layers. Selection of the host substrate in cases of direct wafer bonding to obtain the desired properties is a critical teaching. Additional embodiments include positioning the wafer bond interface within the DBR.

Figure 1 illustrates the theoretical reflectivity vs. wavelength for AlN/GaN and $Al_{.30}Ga_{.70}N$/GaN DBRs.

Figures 2A-BB illustrates preferred embodiments of the present invention.

Figures 3A-F pictorially depict the flow chart corresponding to the present invention.

Figures 4A-F pictorially depict an alternate flow chart corresponding to the present invention.

Figure 5 shows a scanning electron microscope (SEM) cross sectional images of the direct wafer bonded interface between a D-DBR deposited on a GaN/Al_2O_3 structure and a GaP host substrate.

Figure 6 shows a SEM cross section of an active region with a deposited D-DBR which was metallic bonded to a host substrate. The substrate has been removed and a second D-DBR deposited on the side of the $Al_xGa_yIn_zN$ active region opposite the first D-DBR.

Figure 7 shows the optical emission spectrum from 400-500nm from the device in described in Figure 6. The modal peaks describe a vertical cavity structure.

Dielectric distributed Bragg reflectors (D-DBR) consist of stacked pairs of low loss dielectrics where one of the pair materials has a low index of refraction and one has a high index of refraction. Some possible dielectric DBR mirrors are based on paired layers of silicon dioxide (SiO_2) with titanium oxide (TiO_2), zirconium oxide (ZrO_2), tantalum oxide (Ta_2O_5), or hafnium oxide (HfO_2) can achieve the high reflectivities required for a blue vertical cavity surface emitting laser (VCSEL) e.g. > 99.5%, or resonant cavity light emitting device (RCLED), e.g. ~60% or higher. The SiO2/HfO2 stacked pairs are of special interest since they can be used to produce mirror stacks with reflectivities in excess of 99% in the wavelength range of 350-500nm. D-DBRs made with alternating layers of SiO_2 and HfO_2 have been shown to be mechanically stable up to 1050°C, lending flexibility to subsequent processing.

A preferred embodiment is shown in Figure 2. In Figure 2, a first mirror stack 14 e.g. a DBR of high reflectivity, is attached to a suitable substrate. The mirror stack 14 can consist of one or more of the following materials: dielectric, semiconductor and metal. The first mirror stack 14 is wafer-bonded to a top p-layer 18b in an $Al_xGa_yIn_zN$ active region 18 grown on a sacrificial substrate. The $Al_xGa_yIn_zN$ vertical cavity optoelectronic structure 18 has been designed for high gain at the desired wavelength. The wafer bonded interface 16 must be of excellent optical quality with very low scattering. The wafer bonded interface 16 may include an optional intermediate bonding layer (not shown). An optional second mirror stack 20, e.g. a D-DBR (shown in Figure 2), is attached to the $Al_xGa_yIn_zN$ vertical cavity optoelectronic structure 18 on a side opposing the first mirror stack 14. The optional second mirror stack 20 and n- and p-type 18a, 18b layers of the $Al_xGa_yIn_zN$ active region 18 may be patterned and etched to provide areas for ohmic contacts. For a VCSEL, the mirror must have very high reflectivity >99%. For an RCLED, the reflectivity requirement of the mirror(s) is relaxed (>60%).

An alternate approach is for the mirror stack 14 to be attached to the $Al_xGa_yIn_zN$ active region. The wafer bond interface 16 is then between the mirror stack 14 and the host substrate 12. This structure may also have an optional second mirror stack 20. Yet

another approach, to be used in conjunction with either of the first two, is to have a direct wafer bond in the middle of one or both of the mirror stacks. Several possible locations of a wafer bonded interface 16 are shown in Figure 2.

Current constriction may be achieved in either the n-type or p-type active region material by inserting an $Al_xGa_yIn_zN$ layer that may be etched and/or oxidized to improve current and optical confinement and thus reduce lasing threshold or improve device efficiency. Incorporation of such a layer is important when a D-DBR and/or un-doped semiconductor DBR is used since no current is conducted through them. The cavity may be a single or multiple-wavelength cavity depending on the required thickness of the contacting layers to obtain a suitably low forward voltage. Many variations on the structures described above are possible. A similar structure can also be produced with the p- and n-type materials switched.

Figures 3A-F pictorially depict a flow chart corresponding to an embodiment of the present invention. In Figure 3A, a $Al_xGa_yIn_zN$ active region is fabricated on a sacrificial substrate, e.g. Al_2O_3. In Figure 3B, a first mirror stack is attached to a host substrate. Techniques for attaching include bonding, depositing, and growing. In Figure 3C, the first mirror stack is attached via wafer bonding to the $Al_xGa_yIn_zN$ active region. For a VCSEL, direct wafer bonding should be used since it is critical to have low optical losses. In Figure 3D, the sacrificial substrate is removed. In Figure 3E, the optional second mirror stack is attached to the top of the $Al_xGa_yIn_zN$ active region. In Figure 3F, electrical contacts are added to the optional second mirror stack or $Al_xGa_yIn_zN$ active region. Patterning to define the device area and to expose the contact layers can also be performed in the process flow.

Figure 4A-F pictorially depict an alternate process flowchart. In Figure 4A, a $Al_xGa_yIn_zN$ active region is grown over on a sacrificial substrate. In Figure 4B, the first mirror stack is attached to the $Al_xGa_yIn_zN$ active region. In Figure 4C, a host substrate is attached via direct wafer bonding or metallic bonding to the first mirror stack. Since the wafer bond is outside of the optical cavity, losses due to the wafer bond are less critical. In Figure 4D, the sacrificial substrate is removed. In Figure 4E, the optional second mirror stack is attached to the $Al_xGa_yIn_zN$ active region. In Figure 4F, electrical contacts are added to the optional second mirror stack or $Al_xGa_yIn_zN$ active region. Patterning to

define the device area and to expose the contact layers can also be performed in the process flow.

The choice of host substrate for direct wafer bonding is critical and is effected by several properties: mass transport, compliancy, and stress/strain relief. The host substrate can be selected from a group that includes gallium phosphide (GaP), gallium arsenide (GaAs), indium phosphide (InP), or silicon (Si). For Si, the preferred thickness of the substrate is between 1000Å and 50μm.

Mass transport plays an important role in direct wafer bonding. In standard III-V to III-V direct wafer bonding, or III-V to dielectric bonding, at least one surface exhibits significant mass transport at temperatures sufficiently low to preserve the quality of the layers. In contrast, $Al_xGa_yIn_zN$ and most dielectric materials do not exhibit significant mass transport at temperatures consistent with maintaining integrity of the high-In containing $Al_xGa_yIn_zN$ active layers (<1000°C). Lack of mass transport in one or both of the bonding materials impedes wafer adhesion. A model for this is that when both materials exhibit significant mass transport at the bonding temperature, the bonds of both materials can rearrange into the strongest bond across the interface. When only one material exhibits significant mass transport, the bonds of only this one material can align with the surface bonds of the other material. It is difficult in this situation to form a wafer bond of high mechanical strength.

Compliancy is the ability of the material to change shape on an atomic or macroscopic scale to accommodate strains and stresses. For the purposes of this invention, compliancy is defined to be accomplished by materials that have a melting point less than the bonding temperature, or when materials have a ductile/brittle transition below the bonding temperature, or when the substrates are thinner than ~50μm.

Standard III-V wafer bonding for substrates of GaP, GaAs, and InP is generally performed at temperatures of 400-1000°C where both substrates are compliant. Compliancy of at least one of the bonding materials is essential to wafer bonding since the materials have inherent surface roughness and/or lack of planarity on either and microscopic or macroscopic scale. At a temperature of 1000°C a $Al_xGa_yIn_zN$ structure annealed in an N_2 ambient for 20 minutes results in a reduction of PL intensity of approximately 20%. Thus it is desirable to keep the bonding temperature below 1000°C.

GaN-based materials grown on Al_2O_3 substrates are not compliant at bonding temperatures below 1000°C. Dielectric materials that are used to make high reflectivity D-DBRs for wide band-gap semiconductors are typically not compliant below 1000°C. Hence, it is important that the bonding/support substrate and/or intermediate bonding be compliant at those temperatures.

Melting point is one property that determines the compliancy of materials. For example, for the following materials, GaAs (T_m=1510K), GaP (T_m=1750K), and InP (T_m=1330K), it can be seen that the relative order of compliancy is InP, GaAs, GaP, with InP being the most compliant. Materials generally undergo a ductile/brittle transition below the melting point. The compliancy of these materials at high temperatures has to be balanced with desorption of one of the elements. Even though InP is compliant at 1000°C, the material would be severely decomposed at that temperature because of the desorption of phosphorus. Bonding with such materials should be limited to temperatures less than approximately two times the desorption temperature at the ambient pressure during bonding. Thus, the selection of materials must be compatible both with the required compliancy and the bonding temperature.

Very thin substrates can also be compliant. Thin silicon, e.g. < 50μm, is compliant because, even at a high radius of curvature, the stresses are small if the substrate is thin. This technique works well for materials having a high fracture hardness, e.g. silicon (11270 N/mm^2) or $Al_xGa_yIn_zN$. However, materials that have a low fracture hardness, e.g. GaAs (2500 N/mm^2) can easily fracture upon handling. For silicon having a thickness >50μm, even a small radius of curvature causes high stresses in the material, causing the material to fracture. The same applies to other materials that are potential substrate candidates.

Stress and strain relief is exacerbated by the high mismatch strain in GaN grown on Al_2O_3 as well as the coefficient of thermal expansion (CTE) mismatch between $Al_xGa_yIn_zN$ and most other suitable support substrate materials. In contrast to other semiconductor materials that are wafer bonded, the CTE mismatch between $Al_xGa_yIn_zN$ and other semiconductor materials is greater; the stresses are compounded by the different CTE mismatch along the a and c planes of the wurzite material. The stresses in GaN (CTE=5.59, a-plane/3.17x10^{-6}, c-plane/°C) wafer bonded to a different substrate

(GaAs CTE=5.8, GaP CTE=6.8, InP=4.5x10^{-6}/C) necessitates local stress relief since the CTE mismatch of the host substrate should closely match those of both GaN planes. This stress can be accommodated in a compliant material, in an intermediate bonding layer that is soft or a liquid at the bonding interface at the bonding temperature, or by providing local strain relief, e.g. patterning at least one of the bonded interfaces. The intermediate bonding layer is selected from a group that includes dielectrics and alloys containing halides (e.g. CaF_2), ZnO, indium (In), tin (Sn), chrome (Cr), gold (Au), nickel (Ni), copper (Cu), and II-VI materials.

Current spreading is another major concern for GaN-based devices. Lateral current spreading in the p-type material is ~30x less than that in the n-type material. While fabricating high reflectivity mirrors on both sides of the active layer is necessary for a good cavity, the problem of lateral p-layer current spreading is exacerbated because of the insulating nature of the D-DBRs. One way to improve the current spreading in the p-layer is to make a composite DBR of conductive transparent semiconductor and dielectric stacks. The semiconductor part of the stack improves current spreading by adding thickness to the p-layers while the dielectric stack improves the low semiconductor reflectivity to bring the total mirror reflectivity above 99%. This same procedure could be applied to the n-type mirror, though it is less crucial because of the higher conductivity of the n-type layers.

The addition of current constriction layers would further improve current spreading by directing the current only into the cavity, and may be necessary for a VCSEL. This can be applied to the vertical cavity optoelectronic structure with or without a composite semiconductor/dielectric DBR, and may be incorporated into the semiconductor part of a composite mirror. Although the current constriction layers may be included in both the p- and n-layers of the confining layers, it is most effective in the p-confining layers because of the lower conductivity.

The support substrate is necessary if a D-DBR is to be attached to both sides of the active region, since the original host substrate must be removed. There are several methods for removing the sapphire substrate, which is typically employed as a growth substrate. The methods outlined below are only a subset of the techniques that could be used to remove the growth substrate, which can also be a material other than sapphire.

In laser melting, a technique as disclosed by Wong, et al, and Kelley, et al., having a laser with a wavelength for which the sapphire substrate is transparent but the semiconductor layer adjacent the substrate is not, illuminates the back (sapphire side) of the structure. The laser energy cannot penetrate the adjacent semiconductor layer. If the laser energy is sufficient, the semiconductor layer adjacent the sapphire substrate heats to the point that it decomposes. For the case where GaN is the layer adjacent the sapphire substrate, the layer at the interface decomposes into Ga and N, leaving Ga behind at the interface. The Ga metal is then melted and the sapphire substrate is removed from the rest of the layer structure. The decomposition of the layer adjacent the sapphire substrate depends on laser energy, wavelength, material decomposition temperature, and the absorption of the material. The sapphire substrate may be removed by this technique to allow a D-DBR to be attached to the other side of the active region. However, it is critical that the VCSEL interfaces be minimally lossy (<0.5%) and very smooth to maximize cavity resonance characteristics. This laser melting technique has many design variables that may make the laser interface lack the flatness necessary for a VCSEL. Additionally, VCSELs have very tight thickness constraints. There are several ways that laser melting can be used to alleviate both of these problems.

The layer adjacent the sacrificial growth substrate is defined to be a sacrificial layer if the thickness of the layer is such that it will be completely decomposed by the laser. Published results in the literature (Wong, et al.) indicate that a layer thickness that will be completely decomposed is approximately 500Å, but this value will be dependent on the laser energy, the laser wavelength, and material decomposition temperature and the absorption of the layer adjacent the substrate. The layer adjacent the sacrificial layer (opposite the substrate), the stopper layer, is chosen to have a higher decomposition temperature or lower absorption at the laser wavelength than sacrificial layer. The stopper layer, because it has a higher decomposition temperature or low absorption, will not be significantly affected by the laser energy. In this structure, the sacrificial layer is decomposed by the laser, leaving an abrupt interface at the stopper layer which has a higher decomposition temperature or lower absorption. That stopper layer can also then be subsequently etched, oxidized and etched, or decomposed using a laser with different energy and wavelength.

The preferred layer combinations are GaN/$Al_xGa_{1-x}N$, InGaN/ $Al_xGa_{1-x}N$, and InGaN/GaN. In the case of GaN/ $Al_xGa_{1-x}N$ combination, the GaN sacrificial layer will decompose with the laser but the $Al_xGa_{1-x}N$ stopper layer will be unaffected. The $Al_xGa_{1-x}N$ can then be etched away using selective wet chemical etching to stop on a smooth $Al_xGa_yIn_zN$ interface. Alternatively, if the GaN layer described above is not completely decomposed, the remaining GaN can be etched away. Since a thick buffer layer is needed at the beginning of GaN growth and the VCSEL layer interfaces need to be of controlled thickness and very smooth, this technique can be especially valuable.

The thickness of a particular layer or cavity can be tailored by using one or more sacrificial layers and stopper layers. By laser melting and selective wet chemical etching, layer pairs can be decomposed and etched in sequence until the desire thickness is reached. A preferred layer combination is GaN/ $Al_xGa_{1-x}N$ where the GaN is the sacrificial layer and the $Al_xGa_{1-x}N$ stopper layer can be selectively wet chemical etched.

There are other alternative methods of removing the growth substrate. One method is to use AlN which can be selectively etched using wet chemical etching. AlN may be used as a sacrificial layer where the $Al_xGa_yIn_zN$ layers can be removed from the host substrate by using AlN selective etching to undercut the structure. Alternatively, the AlN layers can be oxidized using a wet oxidation process at elevated temperatures. The AlN-oxide can then be etched away using an etchant, e.g. HF. In another approach, the substrate may be exfoliated, e.g. implanted with a light ion into the material. This creates defects at a certain depth. When the substrate is heated, the material selectively cleaves through the dislocations and the substrate is separated from the active layers. Undercutting a ZnO or other dielectric buffer layer via chemical etchants can also be used to remove the substrate from the $Al_xGa_yIn_zN$ layers. This technique can be applied to 2-D or 3-D growth techniques (e.g. SiO_2 or other dielectric used in ELOG) where the $Al_xGa_yIn_zN$ layer is continuous across the substrate or in patterned areas only.

Dielectric DBRs have been deposited on $Al_xGa_yIn_zN$ active regions grown on sapphire substrates. The DBR/ $Al_xGa_yIn_zN$ active region structure was then wafer bonded to a host substrate. In case 1, the DBR/ $Al_xGa_yIn_zN$ active region structure was direct wafer bonded to a GaP host substrate (see Fig 3). In case 2, the DBR/ $Al_xGa_yIn_zN$ active region structure was wafer bonded to a GaP host substrate via an intermediate

CaF_2 layer (Fig 3, where the intermediate layer is not shown). In case 3, the D-DBR was deposited on a host substrate (GaP) and direct wafer bonded to a $Al_xGa_yIn_zN$ active region (Fig. 4). For cases 1 and 3, the bonded area was much smaller than case 2 since no intermediate layer was used. Figure 5 shows scanning electron microscope (SEM) cross sectional images of the bonded interface for a case 1 structure. The interface is smooth and there are no voids visible at this magnification. In case 4, the DBR/ $Al_xGa_yIn_zN$ active region structure was bonded to a host substrate via a metallic intermediate layer consisting of a CrAuNiCu alloy. Figure 6 shows a SEM cross section of case 4, the sapphire substrate as been removed and a second D-DBR deposited on the side of the $Al_xGa_yIn_zN$ active region opposite the first D-DBR. For all the devices, D-DBR stacks were SiO_2/HfO_2, and the sapphire substrate was removed using the laser melting technique. Figure 7 shows the optical emission spectrum from 400-500nm from the device in described in Figure 6. The modal peaks are characteristic of a vertical cavity structure.

CLAIMS

1. A device comprising:

a substrate;

an $Al_xGa_yIn_zN$ structure (18) including a n-type layer, a p-type layer, and an active layer, positioned proximate to the substrate;

a first mirror stack (14), interposing the substrate and a bottom side of the $Al_xGa_yIn_zN$ structure;

a wafer bonded interface (16), interposing the first mirror stack and a selected one of the substrate and $Al_xGa_yIn_zN$ structure, having a bonding temperature; and

a p and an n contact (22a, 22b), the p contact electrically connected to the p-type layer, the n contact electrically connected to the n-type layer.

2. A device, as defined in claim 1, further comprising:

at least one intermediate bonding layer, adjacent the wafer bonded interface; and

one of the intermediate bonding layer and the substrate is selected to be compliant.

3. A device, as defined in claim 2, wherein the $Al_xGa_yIn_zN$ device (18) is a vertical cavity optoelectronic structure.

4. A device, as defined in claim 3, wherein the $Al_xGa_yIn_zN$ device (18) further including a current constriction layer within the p-type layer.

5. A device, as defined in claim 2, wherein the substrate is compliant and is selected from a group that includes gallium phosphide (GaP), gallium arsenide (GaAs), indium phosphide (InP), and silicon (Si).

6. A device, as defined in claim 2, wherein the intermediate bonding layer is compliant and selected from a group that includes dielectrics and alloys containing halides, ZnO, indium, tin, chrome (Cr), gold, nickel, and copper, and II-VI materials.

7. A device, as defined in claim 2, further comprising a second mirror stack (20) positioned adjacent a top side of the $Al_xGa_yIn_zN$ structure.

8. A device, as defined in claim 7, wherein at least one of the first and second mirror stacks (14, 20) is selected from a group that includes dielectric distributed Bragg reflectors and composite distributed Bragg reflectors.

9. A device, as defined in claim 1, further comprising a second mirror stack (20) positioned adjacent the $Al_xGa_yIn_zN$ structure.

10. A device, as defined in claim 9, wherein at least one of the first and second mirror stacks (14, 20) is selected from a group that includes dielectric distributed Bragg reflectors and composite distributed Bragg reflectors.

11. A device, as defined in claim 1, wherein the $Al_xGa_yIn_zN$ device (18) further including a current constriction layer within the p-type layer.

12. A device, as defined in claim 1, wherein the substrate is compliant and is selected from a group that includes gallium phosphide (GaP), gallium arsenide (GaAs), indium phosphide (InP), and silicon (Si).

13. A device, as defined in claim 1, wherein the $Al_xGa_yIn_zN$ device is a vertical cavity optoelectronic structure.

14. A method for fabricating a $Al_xGa_yIn_zN$ structure, comprising the steps of:

attaching a host substrate to a first mirror stack;

fabricating a $Al_xGa_yIn_zN$ structure on a sacrificial growth substrate;

creating a wafer bond interface;

removing the sacrificial growth substrate; and

depositing electrical contacts to the $Al_xGa_yIn_zN$ structure.

15. A method for fabricating an $Al_xGa_yIn_zN$ structure, as defined in claim 14, wherein the step for removing the sacrificial growth substrate comprises the step of laser melting.

16. A method for fabricating an $Al_xGa_yIn_zN$ structure, as defined in claim 14, further comprising the step of attaching an intermediate bonding layer at the wafer bond interface.

17. A method for fabricating an $Al_xGa_yIn_zN$ structure, as defined in claim 16, wherein one of the host substrate and the intermediate bonding layer is selected to be compliant.

18. A method for fabricating a $Al_xGa_yIn_zN$ structure, as defined in claim 14, further comprising the step of attaching a second mirror stack on top of the $Al_xGa_yIn_zN$ structure.

19. A method for fabricating a $Al_xGa_yIn_zN$ structure comprising the steps of:

fabricating a $Al_xGa_yIn_zN$ structure to a sacrificial growth substrate;

attaching a first mirror stack on top of a $Al_xGa_yIn_zN$ structure;

wafer bonding a host substrate to the first mirror stack to create a wafer bond interface;

removing the sacrificial growth substrate; and

depositing electrical contacts to the $Al_xGa_yIn_zN$ structure.

20. A method for fabricating an $Al_xGa_yIn_zN$ structure, as defined in claim 19, wherein the step for removing the sacrificial growth substrate comprises the step of laser melting.

21. A method for fabricating an $Al_xGa_yIn_zN$ structure, as defined in claim 19, further comprising the step of attaching an intermediate bonding layer at the wafer bond interface.

22. A method for fabricating an $Al_xGa_yIn_zN$ structure, as defined in claim 19, wherein one of the host substrate and the intermediate bonding layer is selected to be compliant.

23. A method for fabricating a $Al_xGa_yIn_zN$ structure, as defined in claim 19, further comprising the step of attaching a second mirror stack on top of the $Al_xGa_yIn_zN$ structure.

24. A wafer bonded device substantially as herein described with reference to each of the accompanying drawings.

25. A method for manufacturing a $Al_xGa_yIn_zN$ structure substantially as herein described with reference to each of the accompanying drawings.

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Application No: GB 0002759.9 **Examiner:** Claire Williams
Claims searched: all **Date of search:** 12 May 2000

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1K (KEAX, KELF, KELQ, KELS, KELX, KPXDB)

Int Cl (Ed.7): H01L(21/18, 21/20, 33/00) H01S(5/10, 5/183, 5/187)

Other: ONLINE: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A, P	GB 2333895 (MITEL) WHOLE DOCUMENT, IN PARTICULAR Figures 2a -2i, and page 4 line 27 to page 7 line 2.	
Y	GB 2307791 (HEWLETT -PACKARD) whole document.	1 - 5 and 7 -13
A, P	EP 0896405 A1 (CANON) whole document	
Y	EP 0860913 A1 (MOTOROLA) whole document, in particular claim 8	1 -3, 5, 7-10, 12, 13, 14, 16 - 19
Y	US 5804834 (SHIMOYAMA) whole document, in particular column 2 lines 10 to 12 and 26 to 29.	1-5 and 7 to 13

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